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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,882	09/13/2000	Frank Preiss	99P7765US01	7076

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EXAMINER	
MEW, KEVIN D	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	09/660,882	PREISS, FRANK
	Examiner	**Art Unit**
	Kevin Mew	2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 September 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-10 and 12-18* is/are pending in the application.

4a) Of the above claim(s) *3, 7, 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8-10 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Action

Response to Amendment

1. Applicant's arguments filed on 9/23/2004 regarding claims 1-2, 4-6, 8-10, 12-17 have been considered. Newly added claim 18 has also been considered and is currently pending in the application. Claims 3, 7, and 11 have been canceled by the Applicant.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 5, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anandakumar et al. (USP 6,574,213)

Regarding claim 1, Anandakumar discloses a processor for use in a Voice-over-Internet Protocol telephone (DSP, see Fig. 15), including:

a Voice-over-Internet Protocol processor core operable to transmit computer data and voice data over a computer network (voice samples are supplied from a analog to digital converter to a PCM interface of the DSP and converted to pulse code modulation and then the DSP outputs voice packets and DSP also supports video, real-time control measurement data, see lines 50-66, col. 35 and elements 1515, 1591, 1517, 1595, 1521, 1531, 1593, 1541, 1551, 1555, 1561, 1581, 1583, 1585, 1571, and MCU I/F driver together are interpreted as the VoIP processor core, Fig. 15);

a bus (see element 1771, Fig. 17) on which signals internal to the processor (see element 1751, Fig. 17) are routed;

memory (RAM, see element 1761, Fig. 17) coupled to the Voice-over-Internet Protocol processor core (DSP 1, see element 1751, Fig. 17) through the bus (see lines 61-67, col. 3 and element 1771, Fig. 17);

one or more communication ports (PCM interface, see element 1515, Fig. 15) coupled to the Voice-over-Internet Protocol processor core (see all other elements of DSP) and memory (RAM, see element 1761, Fig. 17) through the bus (see lines 61-67, col. 3 and element 1771, Fig. 17),

wherein the Voice-over-Internet Protocol processor core transmits the computer data and the voice data (voice samples are supplied from a analog to digital converter to a PCM interface of the DSP and converted to pulse code modulation and then the DSP outputs voice packets and DSP also supports video, real-time control measurement data, see lines 50-66, col. 35 and elements 1515, 1591, 1517, 1595, 1521, 1531, 1593, 1541, 1551, 1555, 1561, 1581, 1583, 1585, 1571, and MCU I/F driver together are interpreted as the VoIP processor core, Fig. 15) through the one or more communication ports PCM interface, see element 1515, Fig. 15), and wherein the one or more communication ports are integrated onto a same chip (PCM interface is integrated on the DSP, see Fig. 15) as the Voice-over-Internet Protocol processor core (see all other elements of the DSP, Fig. 15).

Anandakumar does not explicitly show the processor comprises the one or more communication ports that are IEEE 802.3 media access controllers (MACs). However, Anandakumar discloses an on-chip peripheral serial port (see lines 38-39, col. 35) and the DSP is

coupled to a protocol stack that supports Ethernet/MAC (see elements 1511 and 1811, Fig. 18). Moreover, it is well-known in the art that one of the Ethernet standards is IEEE 802.3. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention that the one of the peripheral serial ports supported by the VoIP processor is a standard IEEE 802.3 compliant MAC port such as the serial port and Ethernet/MAC support by the VoIP processor. The motivation to do so is to provide the capability for the VoIP processor to support the well-known IEEE 802.3 Ethernet/MAC port to provide data communication transport interface with a local area network because it will create a network interface for the VoIP processor to transmit data to and receive data from a physical network medium.

Anandakumar does not explicitly show one or more IEEE 802.3 media access controllers (MACs) are integrated onto a same chip.

However, Anandakumar discloses various parts of functions of the DSP and Microcontroller (MCU; note that MCU comprises a MAC protocol layer that MCU is interpreted as a MAC controller, see Fig. 18) can be partitioned and stored on-chip as desired (see col. 39, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the VoIP processor of Anandakumar with the teaching of Anandakumar such that the MCU controller 1781 and DSP processor 1511 are integrated onto the same chip. The motivation to do so is to consolidate both the VoIP processing and physical network interfacing functions in the same chip so that the data and signaling communication overhead time between the MAC controller and DSP within the same chip will be shorter than

that of the situation when MAC controller and the DSP are located on two separate physical chips.

Regarding claim 2, Anandaktumar discloses the processor of claim 1, wherein the one or more communication ports further include one or more pulse code modulation (PCM) ports (see element 1515, Fig. 15).

Regarding claim 5, Anandakumar discloses the processor of claim 1, wherein the one or more communication ports allow the Voice-over-Internet Protocol processor core to be coupled to one or more external components without external interfacing circuitry (see PCM interface, which couples to analog to digital converter (ADC), is integrated on the same DSP processor core, see lines 50-52, col. 35 and Fig. 5).

Regarding claim 18, Anandakumar discloses the processor of claim 1, further comprising a repeater (an echo canceller for removing interference and a gain control that restrengthens signals, see 1517, 1521, Fig. 15; note that it is interpreted that a repeater is a combination of echo canceller and gain control here) coupled to the Voice-over-Internet Protocol processor core through the bus (echo canceller and gain control are coupled to the VoIP processor), wherein the repeater is integrated onto the same chip as the Voice-over Internet Protocol processor core (echo canceller and gain control are on the same chip as the VoIP processor core, see Fig. 15).

3. Claims 4, 6, 8-9, 10, 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anandakumar as applied to claim 1 above, and further in view of Zimmerman et al. (US Patent 6,526,131).

Regarding claim 4, Anandakumar discloses all the aspects of the claimed invention set forth in the rejection of claim 1 above, except fails to explicitly disclose that the one or more communication ports further include one or more universal serial bus (USB) ports.

However, Zimmerman discloses a connectivity box (a processor), which comprises of a processor subsystem and memory, would accept VoIP calls (see lines 24-26, col. 22) and comprises a USB peripheral connect interface (see lines 66-67, col. 7 and lines 1-4, col. 8) to devices such as scanner and printer (see element 31, Figure 2).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Anandakumar such that one or more of integrated communication ports enclosed therein would be USB ports such as the USB ports of the VoIP processor taught by Zimmerman. The motivation to do so is to provide the capability for the VoIP processor to support USB ports because it would allow the VoIP telephone to connect to some USB compatible peripheral devices such as scanners or printers.

Regarding claim 6, Anandakumar discloses an apparatus, comprising: a Voice-over-Internet Protocol processor core operable to transmit computer data and voice data over a computer network (voice samples are supplied from a analog to digital converter to a PCM interface of the DSP and converted to pulse code modulation and then the DSP outputs voice packets and DSP also supports video, real-time control measurement data, see lines 50-66, col.

35 and elements 1515, 1591, 1517, 1595, 1521, 1531, 1593, 1541, 1551, 1555, 1561, 1581, 1583, 1585, 1571, and MCU I/F driver together are interpreted as the VoIP processor core, Fig. 15).

The single-chip Voice-ever-Internet Protocol network processor of Anandakuma does not explicitly disclose a flexible peripheral interconnect (FPI) bus is included in the VoIP processor.

However, Anandakumar discloses the VoIP DSP comprises three data memory buses and on-chip peripherals (see lines 19-27, col. 35). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to combine the peripherals with the data bus of Anandakumar such that one or more of communication peripheral ports integrated onto the single chip of Anandakumar's VoIP processor would be connected to a data bus. The motivation to do so is to allow all the peripheral ports to connect together via the peripheral bus and to receive the information shared on the bus because it would save the space required when connecting all the ports together in the VoIP processor.

Anandakumar does not explicitly show one or more media access controllers (MACs) are integrated onto a single chip through the FPI bus.

However, Anandakumar discloses various parts of functions of the DSP and Microcontroller (MCU; note that MCU comprises a MAC protocol layer that MCU is interpreted as a MAC controller, see Fig. 18) can be partitioned and stored on-chip as desired (see col. 39, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the VoIP processor of Anandakumar with the teaching of

Anandakumar such that the MCU controller 1781 and DSP processor 1511 are integrated onto the same chip. The motivation to do so is to consolidate both the VoIP processing and physical network interfacing functions in the same chip so that the data and signaling communication overhead time between the MAC controller and DSP within the same chip will be shorter than that of the situation when MAC controller and the DSP are located on two separate physical chips.

The single-chip Voice-ever-Internet Protocol network processor of Anandakumar discloses peripherals on-chip, except fail to explicitly disclose that the one or more communication ports are universal serial bus (USB) ports are integrated onto the processor through the FPI bus.

However, Zimmerman discloses a connectivity box (a processor), which comprises of a processor subsystem and memory, would accept VoIP calls (see lines 24-26, col. 22) and comprises a USB peripheral connect interface (see lines 66-67, col. 7 and lines 1-4, col. 8) to devices such as scanner and printer (see element 31, Figure 2).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Anandakumar such that one or more of communication ports integrated onto the single chip of Anandakumar's VoIP processor through the FPI bus would be USB ports such as the USB ports of the VoIP processor taught by Zimmerman. The motivation to do so is to provide the capability for the VoIP processor to support USB ports because it would allow the VoIP telephone to connect to some USB compatible peripheral devices such as scanners or printers.

Regarding claim 8, Anandakumar et al. discloses the apparatus of claim 6, wherein the single-chip Voice-lover-Internet Protocol network processor (DSP, see Fig. 15) further includes one or more pulse code modulation (PCM) ports integrated onto the single chip (see element 1515, Fig. 15) through the FPI bus (peripherals on-chip host-port interface).

Regarding claim 9, Anandakumar discloses the apparatus of claim 8, wherein each PCM port is operable to handle up to 30 time slots (24 time slots, see line 34, col. 28) and wherein each time slot is capable of handling a 64K bit/sec voice channel (PCM is 64kbps, see lines 62-63, col. 24).

Regarding claim 10, Anandakumar discloses an apparatus, comprising: a Voice-over-Internet Protocol processor core operable to transmit computer data and voice data over a computer network (voice samples are supplied from a analog to digital converter to a PCM interface of the DSP and converted to pulse code modulation and then the DSP outputs voice packets and DSP also supports video, real-time control measurement data, see lines 50-66, col. 35 and elements 1515, 1591, 1517, 1595, 1521, 1531, 1593, 1541, 1551, 1555, 1561, 1581, 1583, 1585, 1571, and MCU I/F driver together are interpreted as the VoIP processor core, Fig. 15), the single-chip Voice-ever-Internet Protocol network processor including a memory unit (program spaces) coupled to the Voice-over-Internet Protocol network processor, the memory unit operable to store programs used by the Voice-over-Internet Protocol network processor (store program instructions, see lines 28-33, col. 35).

The single-chip Voice-ever-Internet Protocol network processor of Anandakumar does not explicitly disclose a flexible peripheral interconnect (FPI) bus is included in the VoIP processor.

However, Anandakumar discloses the VoIP DSP comprises three data memory buses and on-chip peripherals (see lines 19-27, col. 35). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to combine the peripherals with the data bus of Anandakumar such that one or more of communication peripheral ports integrated onto the single chip of Anandakumar's VoIP processor would be connected to a data bus. The motivation to do so is to allow all the peripheral ports to connect together via the peripheral bus and to receive the information shared on the bus because it would save the space required when connecting all the ports together in the VoIP processor.

The single-chip Voice-ever-Internet Protocol network processor of Anandakumar discloses peripherals on-chip, except fails to explicitly disclose that the one or more communication ports are universal serial bus (USB) ports are integrated onto the processor through the FPI bus.

However, Zimmerman discloses a connectivity box (a processor), which comprises of a processor subsystem and memory, would accept VoIP calls (see lines 24-26, col. 22) and comprises a USB peripheral connect interface (see lines 66-67, col. 7 and lines 1-4, col. 8) to devices such as scanner and printer (see element 31, Figure 2).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Anandakumar such that one or more of

communication ports integrated onto the single chip of Anandakumar's VoIP processor through the FPI bus would be USB ports such as the USB ports of the VoIP processor taught by Zimmerman. The motivation to do so is to provide the capability for the VoIP processor to support USB ports because it would allow the VoIP telephone to connect to some USB compatible peripheral devices such as scanners or printers.

Anandakumar does not explicitly show one or more media access controllers (MACs) are integrated onto the single chip through the FPI bus.

However, Anandakumar discloses various parts of functions of the DSP and Microcontroller (MCU; note that MCU comprises a MAC protocol layer that MCU is interpreted as a MAC controller, see Fig. 18) can be partitioned and stored on-chip as desired (see col. 39, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the VoIP processor of Anandakumar with the teaching of Anandakumar such that the MCU controller 1781 and DSP processor 1511 are integrated onto the same chip. The motivation to do so is to consolidate both the VoIP processing and physical network interfacing functions in the same chip so that the data and signaling communication overhead time between the MAC controller and DSP within the same chip will be shorter than that of the situation when MAC controller and the DSP are located on two separate physical chips.

Regarding claim 12, Anandakumar discloses the system of claim 10, wherein the single-chip Voice-lover-Internet Protocol network processor (DSP, see Fig. 15) further includes one or more pulse code modulation (PCM) ports integrated onto the single chip (see element 1515, Fig. 15) through the FPI bus (peripherals on-chip host-port interface).

Regarding claim 13, Anandakumar discloses the system of claim 12, wherein each PCM port is operable to handle up to 30 time slots (24 time slots, see line 34, col. 28) and wherein each time slot is capable of handling a 64K bit/sec voice channel (PCM is 64kbps, see lines 62-63, col. 24).

Regarding claim 14, Anandakumar the system of claim 12, further comprising a digital-to-analog/analog-to-digital (DA/AD) converter connected to the single-chip Voice-over-Internet Protocol network processor through one of the one or more pulse code modulation (PCM) ports integrated onto the single chip (see lines 50-52, col. 35 and lines 32-38, col. 36).

Regarding claim 15, Anandakumar the system of claim 14, further comprising a microphone (see lines 30-31, col. 40 and it is inherent that a mobile terminal gas a microphone, see element 1921, Fig. 19), a speaker (it is inherent that a handset has a speaker, see lines 14-17, col. 42 and element 1921, Fig. 19), and a handset (see element 1921, Fig. 5), each connected to the single-chip Voice-over-Internet Protocol network processor through the DA/AD converter (see lines 50-52, col. 35 and lines 32-38, col. 36).

4. Claims 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anandakumar in view of Zimmerman, and in further view of Edholm (USP 6,449,269).

Regarding claim 16, Anandakumar discloses all the aspects of the claimed invention set forth in the rejection of claim 15 above, except fails to explicitly disclose the system of claim 15, further comprising a keypad interfaced with the single-chip Voice-over-Internet Protocol network processor, the keypad operable to allow a user to dial telephone numbers. However, Edholm discloses a connectivity box (a system) that comprises of a VoIP telephone (see lines 27-30, col. 4 and element 100, Fig. 2) with a keypad operable to allow a user to dial telephone numbers (see lines 18-30, col. 5 and element 250, Fig. 2).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP system of Anandakumar with the VoIP telephone of Edholm such that a keypad is interfaced with the VoIP processor of the VoIP telephone to allow users to enter digit phone numbers such as keypad of the VoIP telephone taught by Edholm. The motivation to do so is to capture user input conveying destination information as well as selectively activate or deactivate advanced calling features such as conference and forward because an user interface is required to allow users to enter both destination phone numbers and control the functional features provided by the VoIP telephone.

Regarding claim 17, Anandakumar discloses all the aspects of the claimed invention set forth in the rejection of claim 16 above, except fails to explicitly disclose the system of claim 16, further comprising a liquid crystal display (LCD) operable to display information entered through the keypad.

However, Edholm discloses a connectivity box (a system) that comprises of a VoIP telephone (see lines 27-30, col. 4 and element 100, Fig. 2) with a LCD display operable to display the digits keyed in via keypad of the IP telephone (see lines 36-52, col. 5 and element 260, Fig. 2).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP system of Anandakumar with the VoIP telephone of Edholm such that a LCD display is interfaced with the VoIP processor of the VoIP telephone to display information entered through the keypad such as LCD display of the VoIP telephone taught by Edholm. The motivation to do so is to provide inexpensive output screen on the IP telephone to display user feedback regarding the digits keyed in via keypad of the IP telephone and/or status of the phone itself because it will reduce the development and manufacturing costs of the IP telephone.

Response to Arguments

5. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-3141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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